REMARKS/ARGUMENTS

1. Claim rejections 35 U.S.C. 102(e)

Claims 1 and 3-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Alexander et al.

Response

Claim 1

Claim 1 has been amended to include the limitation of "each delay cell can be divided into a plurality of delay steps" in order to better illustrate the limitation "wherein each subsequent delay cell comprises a smaller delay step than the current delay cell." That is, a first delay cell is divided into a plurality of delay steps, and a subsequent delay cell is divided into a plurality of delay steps, where **the size of the delay steps of the subsequent delay cell are smaller than the size of the delay steps of the first delay cell.** This is fully supported in specification paragraphs [0021] and [0025]. Alexander claims utilizing a control voltage to set a unit delay time wherein each delay step has **the same unit delay time**. "Each delay element 52a....52z, i.e., each buffer or inverter pair, has a delay time of one unit delay, or tu" [col. 5, lines 43-45]. Therefore, although fewer delay elements can be utilized in subsequent delay cells to obtain a smaller **overall** delay time, the delay time of **each delay element** of the subsequent delay cell is still the same as the delay time of each delay element of the first delay cell. Alexander further claims varying the delay unit time by varying the control voltage, wherein a different control voltage must be utilized to obtain a different delay step time. The present invention divides a first delay cell into the plurality of delay steps and then utilizes a delay control signal to set the size of the delay steps **of the first delay cell only.** The delay steps of **a subsequent delay cell** are then set **according to the size of the first delay cell delay steps,** where the delay steps of the subsequent delay cell are smaller than the delay steps of the first delay cell. In

this way, only one control voltage is utilized to set a plurality of delay steps having different delay times; that is, **each delay element has a different delay time, and only one control signal is used by the control unit to program the delay cells.**

Applicant therefore believes that amended claim 1 has been placed in a position for allowance.

Claims 2-7 are dependent on currently amended claim 1 and should be found allowable if claim 1 is found allowable. Objected to claim 8 is dependent on claim 1, and should therefore also be found allowable if claim 1 is found allowable.

2. Claim rejections U.S.C. 102(e)

Claim 14 is rejected under 35 U.S.C. 102(e) as being anticipated by Okayasu.

Response:

Claim 14 has been amended to include the limitations whereby "each delay cell can be divided into a plurality of delay steps". This limitation is added to better illustrate the limitation "wherein each subsequent delay cell comprises a smaller delay step than the current delay cell." This limitation is also fully supported in specification paragraphs [0021] and [0025]. Okayasu claims a system whereby a first control signal is utilized for programming the delay elements wherein **each delay element will have the same delay time:** "if the period of the referential clock is T, the control signal generating unit 24a generates the first control signal so that each of the voltage-control-type variable delay elements 28 generate the delay amount of T/N" [col. 8, lines 44-47]. Similarly, a second control signal is utilized for programming a second chain of delay elements wherein **each delay element will have the same delay time:** "if the period of the referential clock is T,

the control signal generating unit 24b generates the second control signal so that each of the voltage-control-type variable delay elements 29 generate the delay amount of T/(N+1)" [col. 8, lines 56-60]. In the present invention, the first control signal is utilized for programming the delay time of **only the first delay cell of the first delay chain**, and the delay times of the subsequent delay cells will have increasingly smaller delay times, **according to the first control signal.** Similarly, the second control signal is utilized for programming the delay time of **only the first delay cell of the second delay chain**, and the delay times of the subsequent delay cells will have increasingly smaller delay times, **according to the second control signal.** This limitation cannot be achieved by adding more elements to a delay chain (e.g. first delay cell includes 5 inverters/buffers, second delay cell includes 4 inverters/buffers etc.) as it is the **size** of the delay steps themselves that are altered. Okayasu varies the size of the delay steps by varying the control signal whereas the present invention only utilizes one control signal to obtain delay steps of different sizes. That is, for Okayasu, one control signal can only generate one particular delay time, as detailed above "if the period of the referential clock is T, the control signal generating unit 24a generates the first control signal so that **each** of the voltage-control-type variable delay elements 28 generate the **delay amount of T/N**" [col. 8, lines 44-47]. Okayasu selects how many delay elements are to be used in a combination to obtain a desired delay, where each delay element has **the same delay time.** The present invention utilizes a combination of delay elements, each having **a different delay time**, and all the delay times in a delay chain are set by a control unit, according to one control signal.

Applicant therefore believes currently amended claim 14 has been placed in a position for allowance.

Claim 15 is dependent on currently amended claim 14, and should be found allowable if claim 14 is found allowable.

3. New claims

Claim 16

New claim 16 is added by amending previously presented claim 1 to include the limitations of previously presented claim 2. This is because the prior art of Alexander neither teaches nor suggests utilizing a plurality of latches to latch a delay value of the first delay cell and then output a lock signal to a multiplexer and the remaining delay cells in response to the delay control signal. As stated by the Examiner in the section 'Allowable subject matter', claim 2 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant therefore believes the newly entered claim 16 has been placed in a position for allowance.

Claim 17

Claim 17 is added by amending previously presented claim 1 to include the limitations of original claim 8. This is because the prior art of Alexander neither teaches nor suggests utilizing a delay offset for generating an offset delay signal. As stated by the Examiner in the section 'Allowable subject matter', claim 8 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant therefore believes the newly entered claim 17 has been placed in a position for allowance.

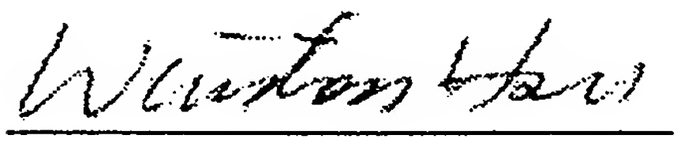
Claim 18

Claim 18 is added by amending previously presented claim 14 to include the limitations of previously presented claim 15. This is because the prior art of Okayasu

neither teaches nor suggests utilizing a plurality of latches for outputting a lock control signal to the remaining delay cells and a multiplexer in response to the first delay control signal and the second delay control signal. As stated by the Examiner in the section 'Allowable subject matter', claim 15 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant therefore believes the newly entered claim 18 has been placed in a position for allowance.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,



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